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10/762,658	01/22/2004	Dean Z. Tsang	TSA-001XX	5151

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EXAMINER	
PHAM, LONG	

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2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/762,658	TSANG, DEAN Z.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/06/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-23,25,26 and 36-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-23,25,26 and 36-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaudhari et al. (US pat 5401714) in combination with Misewich et al. (US patent 6,365,913).

With respect to claim 1, Chaudhari et al. teach a transistor comprising (see figs. 2 and 3A-3B and associated text):

a source 22;

a drain 23;

a gate 25; and

a metal channel 21 having a thickness of less than 5 nm with the channel being positioned relative to the gate such that the carriers in the channel are controlled by the gate.

Chaudhari et al. teach the transistor is a field effect transistor but fail to teach the channel is doped p or hole type.

Misewich et al. teach a field effect transistor having a metal channel which is doped p or hole type or n or electron type to achieve n or p channel FET.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Misewich et al. into the device of Chaudhari et al. to achieve the above benefit.

With respect to claim 2, Chaudhari et al. further teach an insulating layer and a gate insulator 24, the metal channel being positioned between the gate insulator and the insulating layer. See fig. 2 and col. 4, lines 25-26.

With respect to claim 3, Chaudhari et al. fail to teach the substrate is made of silicon.

However, the formation of a FET transistor on a silicon substrate is well-known in semiconductor device.

With respect to claim 4, Chaudhari et al. further teach the metal channel comprises a continuous thin conductive film having a thickness less than 5 nm.

With respect to claim 5, Chaudhari et al. further teach the metal channel has a thickness of 1 nm.

With respect to claim 6, Chaudhari et al. in combination with Misewich et al. further teach the transistor comprises an enhancement mode device.

With respect to claim 7, Chaudhari et al. in combination with Misewich et al. further teach the transistor comprises a depletion mode device.

With respect to claim 16, it is submitted that the channel would inherently have carriers which are inherently controlled by the gate.

With respect to claim 17, Chaudhari et al. in combination with Misewich et al. further teach the source comprises a p-type metal and the drain comprises of a p-type metal and wherein the metal channel is a p-type metal (see fig. 1 and col. 6, lines 40-50 of Misewich et al.). Further since Chaudhari et al. in combination with Misewich et al. further teach the claimed thickness for the metal channel, the carriers would inherently be controlled to form a p-channel depletion-mode device.

With respect to claim 18, Chaudhari et al. in combination with Misewich et al. further teach the source comprises a n-type metal and the drain comprises of an p-type metal and wherein the metal channel is a p-type metal (see fig. 1 and col. 6, lines 40-50 of Misewich et al.). Further since Chaudhari et al. in combination with Misewich et al. teach the claimed device, an n-type inversion layer would inherently be formed on the p-type metal when a positive gate voltage is applied to form an n-channel enhancement mode device.

With respect to claim 19, Chaudhari et al. in combination with Misewich et al. further teach the device comprises of a CMOS device. See col. 6, lines 40-60 of Misewich et al.

With respect to claim 20, the formation of channel having plurality of layers is well-known.

With respect to claim 21, Chaudhari et al. in combination with Misewich et al. further teach the metal channel comprises of metal alloy. See col. 6, lines 40-50 of Misewich et al.

Claims 8, 9, 10, 12-15, 22-23, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al. (US pub 20040169227) in combination with Chaudhari et al. (US pat 5401714), Song et al. (US patent 2004/0149579), and Ogura et al. (US publication 2002/0045319).

With respect to claim 8, Wei et al. teach a field effect transistor device comprising (see figs. 1 and 2A-2B and associated text):

an channel 33 formed over an insulator 30B, the metal channel further comprising a continuous thin conductive film;

a source including a p-type material and a drain including a p-type material (para [0025]); and

a gate 36 and a gate insulator 34 formed over the channel, the gate controlling carriers in the channel.

Wei et al. fail to teach the channel is made of a thin n-type metal layer having a thickness of less than 5 nm.

Chaudhari et al. teach a FET transistor in which a channel is made of a thin n-type metal layer having a thickness of less than 5 nm to achieve a superconductive channel. See figs. 2 and 3A-3B and associated text.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Chaudhari et al. into the device of Wei et al. to achieve the above benefit.

With respect to claim 9, Wei et al. in combination with Chaudhari et al. further teach the insulator further comprises an insulating layer over a substrate 30A, the metal

channel being positioned between the gate and the insulating layer and the gate insulator being positioned under the gate and over the metal channel.

With respect to claim 3, Wei et al. fail to teach the substrate is made of silicon. However, the formation of a FET transistor on a silicon substrate is well-known in semiconductor device.

With respect to claim 12, Wei et al. further teach the device comprises of a CMOS device. See [0007] .

With respect to claim 13, Wei et al. further teach an encapsulation layer 21. See fig. 1.

With respect to claim 14, Wei et al. fail to teach the range for the width of the channel.

Song et al. teach a channel having width of less than 500 nm. See claim 4.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for width of the channel of Song et al. in the device of Wei et al. to achieve the benefit of controlling current flow through the channel by controlling the voltage applied across the channel. See [0005].

Further with respect to claim 14, Wei et al. fail to teach the range of the length of the channel.

Ogura et al. teach a channel having a length of 40 nm to reduce voltage and increase speed. See [0024].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the length of the channel of Ogura et al. in the device of Wei et al. to achieve above advantage.

With respect to claim 15, the formation of channel having plurality of layers is well-known.

With respect to claims 22, 23, and 26, since Wei et al. in combination with Chaudhari et al., Song et al, and Ogura et al. teach the claimed device, a p-type inversion layer would inherently be formed on a side of the n-type metal when a negative gate voltage is applied to form an p-channel enhancement mode device.

Further with respect to claim 25, Since Wei et al. in combination with Chaudhari et al. teach the claimed thickness of the channel layer, it is inherently greater than the thickness of the p-type inversion layer.

Claims 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaudhari et al. (US pat 5401714) in combination with Misewich et al. (US patent 6,365,913).

With respect to claim 36, Chaudhari et al. teach a transistor comprising (see figs. 2 and 3A-3B and associated text):

a source 22;

a drain 23;

a gate 25; and

a metal channel 21 having a thickness of less than 5 nm with the channel being positioned relative to the gate such that the carriers in the channel are controlled by the gate.

Chaudhari et al. teach the transistor is a field effect transistor but fail to teach the channel is a metal alloy doped p or hole type.

Misewich et al. teach a field effect transistor having a metal channel which is a metal alloy doped p or hole type or n or electron type to achieve n or p channel FET.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Misewich et al. into the device of Chaudhari et al. to achieve the above benefit.

With respect to claim 37, Chaudhari et al. further teach an insulating layer and a gate insulator 24, the metal channel being positioned between the gate insulator and the insulating layer. See fig. 2 and col. 4, lines 25-26.

With respect to claim 38, Chaudhari et al. in combination with Misewich et al. further teach the transistor comprises an enhancement mode device.

With respect to claim 39, Chaudhari et al. in combination with Misewich et al. further teach the transistor comprises a depletion mode device.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chaudhari et al. (US pat 5401714) in combination with Misewich et al. (US patent 6,365,913).

With respect to claim 40, Chaudhari et al. teach a transistor comprising (see figs. 2 and 3A-3B and associated text):

A metal channel 21 formed over an insulator;

a source 22 and a drain 23; and a gate 25 and a gate insulator 24 formed over the channel, the gate controlling carriers in the channel.

Chaudhari et al. teach the transistor is a field effect transistor but fail to teach the channel is a metal alloy doped n or electron type.

Misewich et al. teach a field effect transistor having a metal channel which is a metal alloy doped p or hole type or n or electron type to achieve n or p channel FET.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Misewich et al. into the device of Chaudhari et al. to achieve the above benefit.

Chaudhari et al. fail to teach that the source and drain are p type material.

However, the doping of the sources or drain with p type material to allow the formation of n channel FET transistor is well-known in semiconductor art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

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